AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1101] with the following amended paragraph:

[1101] Such channel stripes 402 are preferably formed by depositing an amorphous silicon layer and etching the layer using a channel mask to form the channel stripes and annealing the layer to form a thin film transistor channel. The word line stripes [[106]] 406 may be formed of a stack of more than one layer, such as a polysilicon layer covered by a silicide layer, or may be a three level stack, as shown in the figure.

Please replace paragraph [1102] with the following amended paragraph:

[1102] An interlevel dielectric layer 408 is formed above the word line stripes to isolate the word lines on one level (e.g., word line stripes 406 depicted on level 1) from the channel stripes on the next higher level (e.g., channel stripes ~~402~~ depicted on level 2). A dielectric may also be used to fill spaces between the word line stripes of a given level. As can be appreciated, such a structure forms a plurality of series-connected transistors within each channel stripe 402.